Supply Voltage Dependency on the Single Event Upset Susceptibility of Temporal Dual-Feedback Flip-Flops in a 90 nm Bulk CMOS Process

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***Abstract*—In this paper we investigate the efficiency of using temporal and spatial hardening techniques in flip-flop design for single event upset (SEU) mitigation at different supply voltages. We present three novel SEU tolerant flip-flop topologies intended for low supply voltage operation. The most SEU tolerant flip-flop among the proposed flip-flop topologies shows ability of achieving maximum SEU cross-section below $1.9 \cdot 10^{-10}$ cm^2/bit (no SEUs detected) at 500 mV supply voltage, $4 \cdot 10^{-10}$ cm^2/bit at 250 mV supply voltage, and $2 \cdot 10^{-9}$ cm^2/bit at 180 mV supply voltage. When scaling the supply voltage from 1 V down to 500 mV, 250 mV and 180 mV, the proposed flip-flops achieve at least -72%, -92.5% and -95% (respectively) reduction in energy per transition compared to a Dual Interlocked Storage Cell based flip-flop when operated at a supply voltage of 1 V. The flip-flops have been designed and fabricated in a low-power commercial 90-nm bulk CMOS process and were tested using heavy ions with LET between 8.6 MeV-cm^2/mg and 53.7 MeV-cm^2/mg.**

***Index Terms*—Complimentary metal-oxide semiconductor (CMOS), flip-flop, low power, low voltage, radiation tolerant, single event transient (SET), single event upset (SEU).**

I. Introduction

LOW power electronics have been one of the main focus areas in commercial complimentary metal-oxide semiconductor (CMOS) electronics the last two decades. However, the interest for low power exists also in high reliability application areas such as space applications [1], [2]. The obvious reason for low power electronics being attractive in space applications is the limited power budget in spacecraft, for example when the power supply is dependent on solar cells.

D Flip-flops (DFFs) are fundamental building blocks in sequential CMOS circuits. In sequential CMOS circuits, single event upsets (SEUs) are the main source of radiation induced errors and SEU mitigation techniques often rely on supply voltages being as high as possible in order to attain the best possible SEU tolerance. As supply voltages scale down, internal nodes become more susceptible to SEUs due to the reduction of the critical charge (Qcrit) of the internal nodes [3], [4], [5]. On the other hand, the most direct and dramatic means of reducing the power consumption of an integrated circuit (IC) is by reducing the supply voltage. Power consumption savings up to several orders of magnitude have been achieved, given that the transistors are operated in the subthreshold region [6]. Another benefit of low supply voltage operation is that the Total Ionizing Dose (TID) induced leakage decreases [7]. Low TID induced leakage is important for realizing both low power and reliable ICs.

To the authors' knowledge, this work is the first to investigate the common impact of temporal and spatial hardening techniques on the SEU sensitivity of DFFs, as a function of a wide supply voltage range (180 mV to 1 V). Our results show that temporal hardening has higher impact on the SEU sensitivity of the proposed DFFs at supply voltages above 500 mV, while spatial hardening has higher impact on the SEU sensitivity at supply voltages below 500 mV. Furthermore, we also show that DFFs operated at low supply voltages can have good SEU tolerance at the same time as having increased energy efficiency. One of the proposed DFFs operated at a supply voltage of 500 mV without experiencing any SEUs, and while being 72% more energy efficient than a Dual Interlocked Storage Cell (DICE) DFF at 1 V supply voltage.

The proposed DFF topology is implemented using three different configurations in terms of delay of the temporal elements and separation of the sensitive nodes. The DFFs are compared in terms of area, clk-to-Q delay, setup time, energy per transition and maximum frequency. Furthermore, a DICE-based DFF is also included in this paper in order to serve as a reference DFF. Spectre simulations are used for evaluating the DFF performance and heavy ion radiation testing is used for evaluating the SEU susceptibility of the DFFs.

The rest of this work is organized as follows: Section II describes the relevant radiation effects and previous work. Circuit design and area comparison of the latches are presented in Section III. Section IV presents the circuit performance of the DFFs based on Spectre simulations. The prototype IC, heavy ion test facility, radiation test setup and experimental results are presented in Section V. Section VI presents a discussion on the key topics in this work, followed by the conclusion in Section VII.

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II. Single Event Effects and Previous Work

Typical Single Event Effects (SEE) are single event transients (SET) and SEUs. SETs are transient voltage fluctuations which are induced by charge collection, as a result of an inbound particle interacting with the sensitive nodes (typically reverse biased source/drain), in a transistor [8]. These voltage fluctuations, although short in duration, can propagate to storage elements and cause an erroneous latched logic state, resulting in a SEU. A SEU can be defined as a change in the logic state of a memory element from a logic one to a logic zero or vice-versa. SEUs typically occur when inbound particles alter the voltage in sensitive nodes of memory elements in such a way that it results in a bit error. SEUs are non-destructive events; therefore, the affected logic can be rewritten or reset to regain proper operational behavior. Based on the nature of the SEEs described here, it is apparent that SEUs are a highly relevant topic for memory elements such as Static Random Access Memory (SRAM), latches and flip-flops.

Single event latchup (SEL) is another relevant SEE in this work. Due to utilization of supply voltage below 1.2 V, the probability of SEL occurrences is very low [9]. Nevertheless, SEL was monitored during radiation testing as a precaution.

A. Previous Work

To the authors knowledge, the work presented in [7] is the first to explore the potential benefits of operating radiation tolerant CMOS circuits at supply voltages as low as 500 mV. There it was shown that by reducing the supply voltage and applying body bias techniques, a decrease of TID induced leakage current in a 0.35 μm CMOS n-channel device could be achieved. The reduction of TID induced leakage with reduced supply voltages has later also been verified for 130 nm [10], [11] and for 90 nm [12] CMOS technology nodes. The reason for the reduced impact of TID induced leakage at low supply voltages is the increased recombination of e-h pairs, and thereby less interface traps, in the absence of a strong electric field near the oxide [13].

Reduction of the supply voltage also reduces the parasitic bipolar gain which, together with weaker electric fields, leads to reduced particle induced charge collection [14], [15]. Still, by using Technology Computer Aided Design (TCAD) simulations, it was shown that the particle induced Full Width Half Rail (FWHR) pulsewidth increased considerably with a decrease in the supply voltage [14]. Thereby it was shown that the FWHR pulsewidth is more dependent on the device conductivity than on the electric field and parasitic bipolar gain. However, it has also been shown that if multinode charge collection is taken into consideration, then pulse quenching can be utilized for reducing the FWHR pulsewidth [16], also when the supply voltage is scaled down [15].

Regardless of the increased SET and SEU vulnerability, several works have investigated low supply voltage operation for realizing SEU tolerant, ultra-low power CMOS circuits. The most popular radiation tolerant memory element, which offers a good trade-off between area, power and speed, is the DICE memory element [17]. A DICE storage cell was used in [10] for realizing a 32×18 bit register file in a 130 nm bulk CMOS process. The register file was tested using heavy ions at a supply voltage down to 250 mV, and was found to be SEU free for supply voltages above 450 mV with maximum LET of 44.24 MeV-cm^2/mg. The memory cells were hardened by interleaving of sensitive nodes across multiple bit-cells.

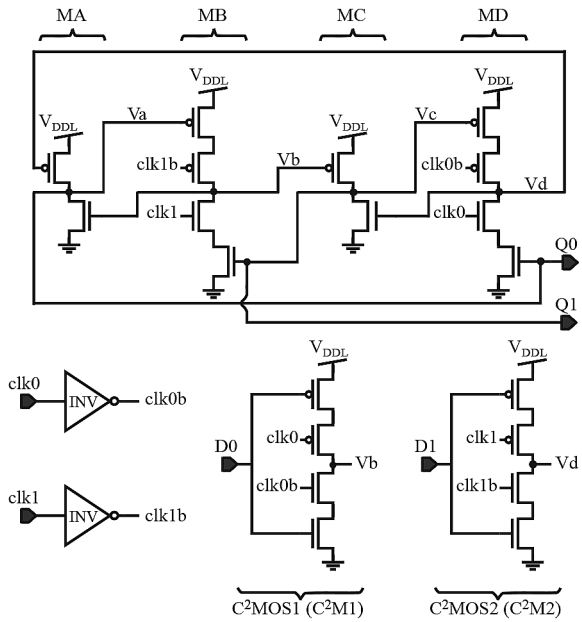

Fig. 1. C^2MOS DICE latch.

In terms of radiation tolerant DFF design, the work presented in [18] and [19] evaluate the heavy ion induced SEU response of radiation tolerant DFFs down to a supply voltage of 700 mV. To our knowledge, this is the lowest supply voltage previously used for assessing the heavy ion induced SEU response of DFFs. In contrast to the previous work, the proposed DFFs are evaluated for deep subthreshold supply voltages down to 180 mV.

III. Circuit Design

In this paper, two DFF topologies have been designed with the aim of investigating their SEU tolerance at different supply voltages. A DICE DFF (Section III-A) was designed in order to serve as a radiation tolerant reference for the proposed Temporal Dual-Feedback (TDF) DFFs (Section III-B). The TDF DFFs were implemented using three different configurations.

All DFFs have been implemented using standard threshold voltages transistors. The threshold voltage ($|V_{th}|$) of the transistors used in both the designs varies between 400 mV to 480 mV depending on configuration (PMOS, NMOS, body effect, etc.). The nominal supply voltage of the process is 1.2 V. All transistor (both PMOS and NMOS) gate lengths have been increased from 90 nm to 150 nm, primarily in order to achieve lower parameter variations and higher $\mathrm{I_{on}-to-I_{off}}$ ratio when operated in the subthreshold region [20]. Sizing was optimized for equal rise/fall times at $\mathrm{V_{DDL}} = 500$ mV.

A. DICE DFF

The C^2MOS DICE DFF in this paper is topologically equivalent to the DFF used in [21] and [22]. The DICE DFF is configured as a master-slave DFF and consists of two identical DICE latches. The DICE latch is shown in Fig. 1.

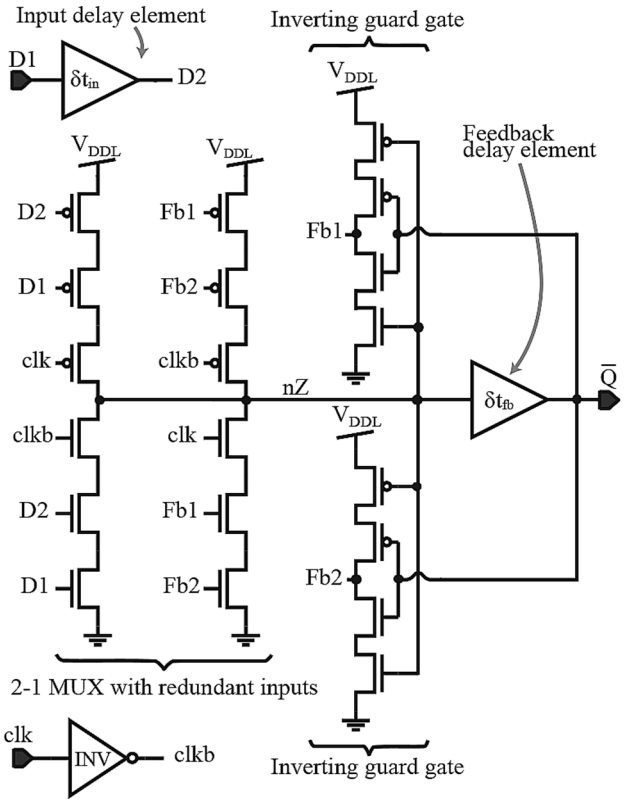

Fig. 2. Transistor-level schematic of the proposed TDF latch.

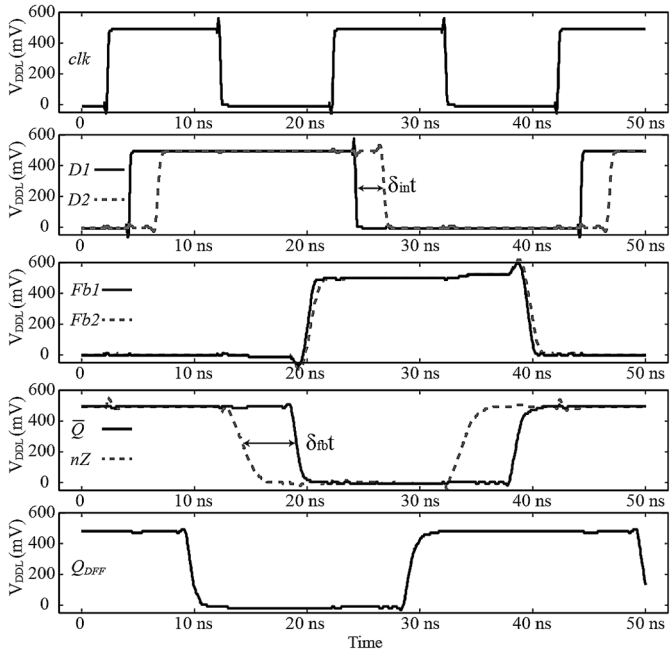

Fig. 3. Waveforms of the TDF latch (top four traces) and DFF output (bottom trace) at $V_{DDL} = 500$ mV.

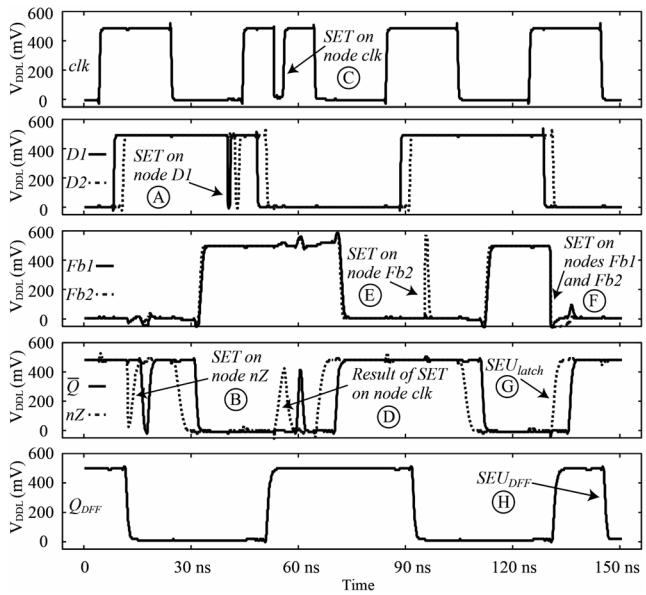

Fig. 4. Waveforms of the TDF master latch (top four traces) and DFF output (bottom trace) at $V_{DDL} = 500$ mV when SETs occur on nodes D1, nZ, Fb2 and Fb1 & Fb2.

DICE latches are inherently insensitive to single-node particle hits on the memory nodes [17]. The DICE part of the latch serves as redundant memory storage where memory nodes Va and Vc have the same logic value and memory nodes Vb and Vd have the same logic value (e.g. Va-Vb-Vc-Vd are 0-1-0-1 or 1-0-1-0). If one of the memory nodes is affected by a particle hit, the unaffected nodes will propagate correct logic values via the state restoring interconnect. For example, state restoring interconnect of node Vc are nodes Vb and Vd. However, if two critical nodes (Va and Vc or Vb and Vd) are affected simultaneously, this would cause the other two memory nodes to flip as well, resulting in an SEU.

Coincidently, even though the DICE incorporates dual redundancy, the internal memory nodes are still susceptible to charge sharing between the sensitive nodes as a result of a single particle strike [23], [24]. Fig. 5 (top left) shows the distance between the sensitive nodes of the DICE latch. In this work, extensive spatial separation of sensitive nodes was not applied and only inter-latch sensitive node interleaving was used, both in the DICE DFF and in the TDF DFFs. Therefore, since the DICE latch is the smallest of the latch implementations in this work, its sensitive nodes (Va to Vc, Vb to Vd) are only separated by minimum of 1.6 μm.

B. TDF DFF

The main principle behind temporal redundancy is to utilize one or more delay elements and connecting the delayed nodes to a voter circuit such as a guard gate (also known as Muller C-elements [25]) or a majority voter. An SET occurring at the input of the delay element arrives at different times at the voter inputs and is thereby prohibited from propagating, given that the SET pulsewidth is smaller than the delay of the delay element(s) [26]. Similar to the temporal DFFs in [27], [28], the proposed DFF utilizes guard gates and delay elements in order to filter out SETs. Other implementations of temporal DFFs use Triple modular redundancy (TMR) at a small expense of area consumption [18], [26].

The proposed DFF is made up of two identical TDF latches in a master-slave arrangement. The TDF latch and its sub-components are shown in Fig. 2 and are as follows: A 2-1 inverting

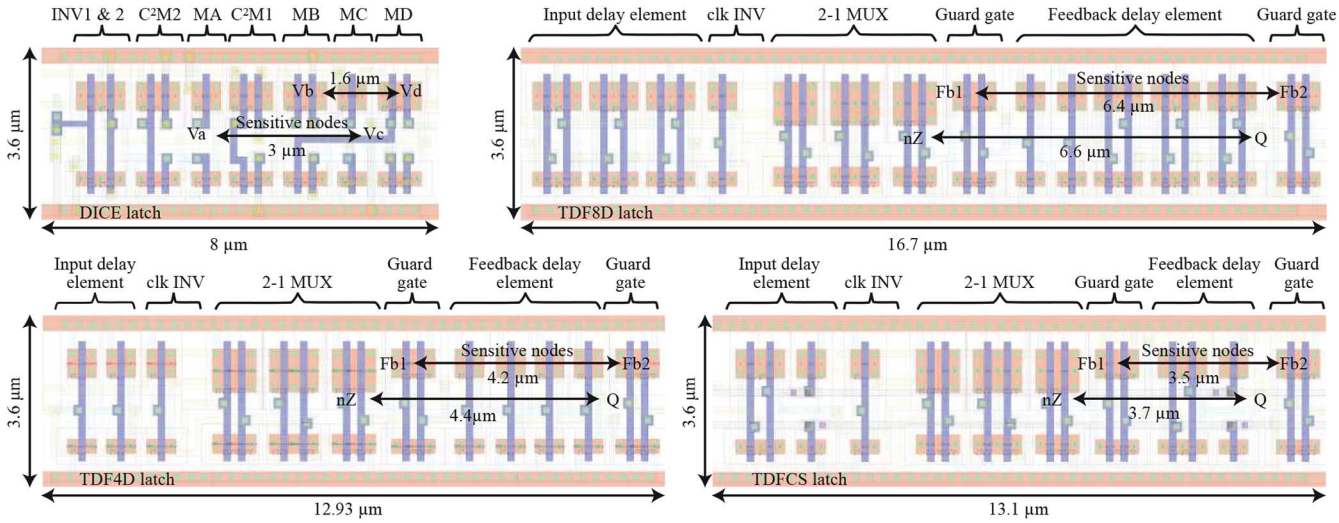

Fig. 5. Area comparison between the implemented latches: DICE (top left), TDF8D (top right), TDF4D (bottom left) and TDFCS (bottom right).

multiplexer (MUX) with redundant inputs, input delay element (with delay duration of δt_{in}), feedback delay element (with delay duration of δt_{fb}) and dual feedback paths in the form of inverting guard gates. What separates the proposed DFF from previously published work such as [18], [26], [28] is that it uses only one delay element in the feedback loops in the latches. Dual feedback loops ensure that the feedback loops do not tri-state during SET recovery (discussed later in this Section), a mechanism which can cause SEUs in latches with single feedback and a single delay element.

Fig. 3 shows a waveform diagram of the functionality of the TDF latch. In the bottom trace, the output of the master-slave TDF DFF is shown. The 2-1 MUX determines if the redundant data input ($D1$ and $D2$) or the redundant feedback ($Fb1$ and $Fb1$) is propagated to the output ($\overline{Q}$), depending on the clock (*clk* and *clkb*). If *clk* is low, the latch is in sample mode, causing $\overline{Q} = \overline{D}$. If clk is high, the latch is in hold mode, causing $\overline{Q} = \overline{Fb}$. When *clk* changes from low to high, $\overline{Fb} = \overline{D}_{(t-1)}$, where $\overline{D}_{(t-1)}$ denotes the state of $\overline{D}$ before *clk* changes value. This yields an inverting D-type latch. Placing two such latches in a master-slave configuration results in a positive edge triggered D-type DFF.

The TDF DFFs are tolerant to single node hits on all internal nodes, as well as on the data and clock inputs. Fig. 4 shows how SETs influence the internal nodes of the TDF latches. In terms of temporal hardening, utilization of only the feedback delay element is sufficient in order to filter out single node SETs in the TDF latch. However, a conservative approach was chosen when implementing the TDF latch, and an input delay element was added to alleviate the SET occurrences at node nZ. This means that SETs with pulsewidth shorter than δt_{in} will be filtered out (mark Ⓐ, in Fig. 4), and SETs with pulsewidth longer than δt_{in} will propagate to node nZ.

An SET occurring at node nZ arrives at the inputs of the guard gates at different times due to the feedback delay element, and is thereby prohibited to propagate to the feedback nodes $Fb1$ and $Fb1$, given that the SET pusewidth is smaller than δt_{fb} (mark Ⓑ, in Fig. 4). The same mechanism is responsible for making the TDF latches tolerant to SETs on the clock input. When the clock network experiences an SET during the hold mode of the latch (mark Ⓒ, in Fig. 4), node nZ experiences a SET induced glitch, which is filtered out by the feedback delay element and the guard gates (mark Ⓓ, in Fig. 4). Similarly, if any of the feedback nodes, $Fb1$ or $Fb1$, experiences an SET, the redundant feedback inputs in the 2-1 MUX ensure that the SET does not propagate to node nZ (mark Ⓔ, in Fig. 4). However, similar to the the DICE latch, the TDF latch has also nodes which are sensitive to charge sharing. If both feedback nodes ($Fb1$ and $Fb2$) experience SETs at the same time (mark Ⓕ, in Fig. 4), an SET induced glitch would occur on node nZ. This glitch causes the guard gates to enter tri-state and thereby prohibits the guard gates from recovering from the SET. This causes an SEU in the latch (mark Ⓖ, in Fig. 4), which causes and SEU in the DFF (mark Ⓗ, in Fig. 4). Therefore, guard gates in the feedback need to be physically separated in order to avoid charge sharing affecting internal nodes ($Fb1$ and $Fb2$) simultaneously. The same applies to the output of the 2-1 MUX and the output of the feedback delay element (nZ and $\overline{Q}$). The sensitive node separation in the TDF DFFs is shown in Fig. 5. The minimum distance between sensitive nodes is 6.4 μm, 4.2 μm and 3.5 μm for the TDF8D, TDF4D and TDFCS, respectively.

Three configurations of the TDF latch have been implemented, each with a different delay element configuration for evaluating the trade-off between SEU mitigation efficiency, area, delay, energy consumption and maximum frequency. The delay elements used in this work are shown in Fig. 6. The TDF8D utilizes six inverters in series for realizing δt_{in} and eight inverters in series for realizing δt_{fb} (Fig. 6(a)). The TDF4D utilizes two inverters in series for realizing δt_{in} and four inverters in series for realizing δt_{fb} (Fig. 6(b)). The number of inverters comprising the delay elements at the input of TDF4D and TDF8D was reduced, since the feedback delay element is the most critical (discussed in Section VI-C). The TDFCS utilizes two current starved inverters in series for realizing both δt_{in} and δt_{fb} (Fig. 6(c)). The current starved inverters are added to the comparison, in order to evaluate

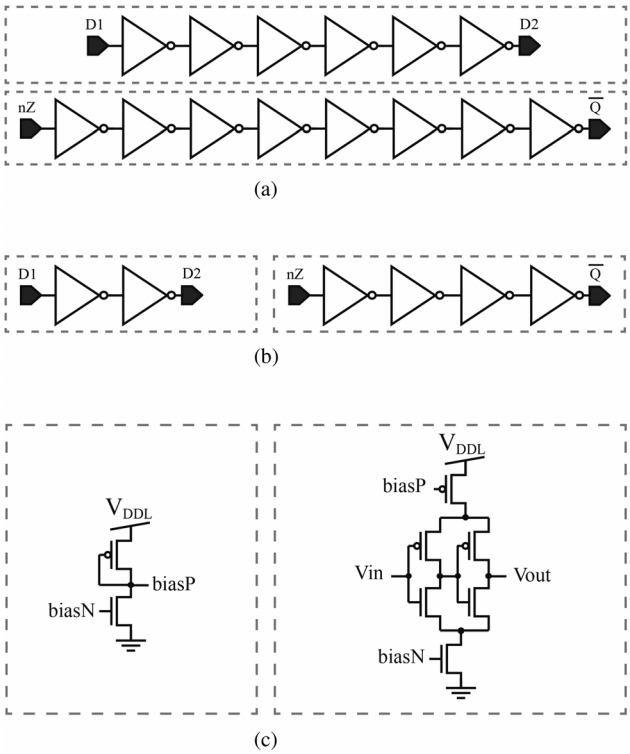

Fig. 6. Delay elements used in the TDF8D (top), TDF4D (middle) and TDFCS (bottom).(a) Input delay element (top) and feedback delay element (bottom) for the TDF8D latch. (b) Input delay element (left) and feedback delay element (right) for the TDF4D latch. (c) Bias circuit (right) and input and feedback delay element (left) for the TDFCS latch.

TABLE I
RELATIVE DFF PERFORMANCE COMPARISOPN

Perf. Metrics	DICE	TDF4D	TDFCS	TDF8D
$t_{clk\text{-}Q}$	1	1.3	1.5	1.8
E_{tr}	1	1	0.9	1.5
t_{setup}	1	10	11	17
f_{max}	1	0.49	0.41	0.32

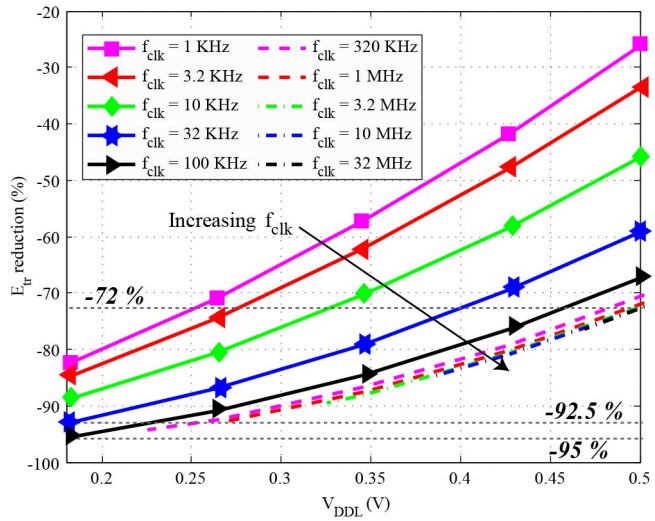

Fig. 7. Switching energy reduction for TDF8D DFF as a function of V_{DDL}, compared to DICE DFF at $V_{DDL} = 1$ V.

if they can be efficient SET filtering elements at low supply voltages. As a result of supply voltage scaling, all delays will vary depending on the supply voltage and additionally the *biasN* voltage for the TDFCS. It has been shown that the SET width increases with decreasing supply voltage [14]. Thereby, utilization of supply voltage dependent delay elements is necessary in order to compensate for increasing SET widths with decreasing supply voltage.

IV. PERFORMANCE SIMULATIONS

Performance of the DICE DFF and the TDF DFFs has been analyzed using post-layout Spectre simulations at 27°C with four inverters as load (FO4). The performance metrics evaluated were energy per transition (E_{tr}), clk-to-Q delay (t_{clk-Q}), setup time (t_{setup}) and maximum frequency (f_{max}).

Table I shows the performance metrics of the TDF DFFs in values normalized to the DICE DFF. The performance metrics of all DFFs in Table I are based on supply voltage sweeps from $V_{DDL} = 180$ mV to $V_{DDL} = 1$ V with clock frequency of 100 kHz. The t_{clk-Q} is the average clk-to-Q delay when the output (Q) goes from 0-1 and from 1-0 at rising edge of the clock (clk). The E_{tr} is defined as the average energy consumed by a DFF during one clock period for all input data patters (0-0, 0-1, 1-0, 1-1) [29]. Both dynamic and leakage energy is taken into account. The t_{setup} is based on when the input (D) is high and $f_{max} = 1/(t_{setup} + t_{clk-Q})$. From Table I, it can be seen the the DICE DFF has a better overall performance than the TDF DFFs. For the TDF DFFs, t_{clk-Q} is dominated by δt_{in} and δt_{fb} of the slave latch (in addition to the delay in the MUX). The dominating factors which influence t_{setup} of the TDF DFFs are δt_{in} and δt_{fb} of the master latch (in addition to the MUX and guard gate). Hold times are also influenced by δt_{in} and δt_{fb}, making the hold times in the TDF DFFs negative. The higher E_{tr} in TDF8D compared to the DICE, TDF4D and TDFCS, is due to utilizing long inverter chains as delay elements.

The inverter based delay elements also contribute to a higher leakage energy, making the relative energy consumption of the TDF8D and TDF4D DFFs increase with decreasing frequencies (see Fig. 7). Fig. 7 shows the E_{tr} reduction for TDF8D DFF as a function of V_{DDL} compared to DICE DFF at $V_{DDL} = 1$ V. When scaling V_{DDL} from 1 V down to 500 mV, 250 mV and 180 mV, the TDF8D DFF achieves at -72%, -92.5% and -95% (respectively) reduction in E_{tr} compared to the DICE DFF when operated at $V_{DDL}1$ V. The performance simulations presented in Table I show that the TDF DFFs may benefit from certain topological changes, which can increase the performance. Possible topological improvements will be discussed in Section VI.

A. Delay Elements in the TDF Latches

Table II shows the simulated (based on post layout simulations) delay of the input delay elements (δt_{in}), and the delay of the feedback delay elements (δt_{fb}), at the supply voltages used in radiation testing. From Table II it can be seen that the delay of all delay elements increases with decreasing supply voltage. The delays of the delay elements comprised of standard inverters are directly set by the supply voltage. On the other hand, the current starved inverter based delay elements are more flexible in terms of the achievable delays by adjusting the bias voltage *biasN*. For

TABLE II
SET FILTERING DELAY AS A FUNCTION OF THE SUPPLY VOLTAGE

DFF topology and delay configuration		V_{DDL} 1 V	0.5 V	0.25 V	0.18 V
TDF4D	δt_{in}	115 ps	830 ps	68.8 ns	360 ns
	δt_{fb}	220 ps	2.47 ns	193 ns	1.01 us
TDFCS	δt_{in}	116 ps	1.63 ns	151 ns	792 ns
	δt_{fb}	222 ps	2.57 ns	208 ns	1.08 us
TDF8D	δt_{in}	213 ps	2.69 ns	221 ns	1.16 us
	δt_{fb}	434 ps	4.38 ns	347 ns	1.85 us

the purpose of the radiation testing, limited beam time did not allow for varying *biasN*, therefore the bias voltage was set to V_{DDL}. Similarly, the supply voltage of the bias circuit was also set to V_{DDL}, which resulted in the delays in Table II.

V. EXPERIMENTAL RESULTS

The experimental results are based on accelerated heavy ion irradiation testing of a 90 nm test IC produced in a commercial low-power process.

A. Prototype IC

The DFFs presented in the paper were used to implement four separate 1024-bit shift registers, one for each of the DFF types in this paper. The DICE shift register employed dual clocks, while the TDF shift registers employed a single clock. The dual clocks were branched out from the single clock at the input of the IC. The data input was common for all shift registers. All shift registers were connected to a dedicated level shifter capable of converting digital input signals at $V_{DDL} = 110$ mV $- 1.2$ V to digital output signals at $V_{DDH} = 1.2$ V. The level shifter used in this test IC is similar to the the level shifter in [30]. The level shifters are connected to digital buffers which were operated at $V_{DDH} = 1.2$ V. The TDF shift registers were functional between $V_{DDL} = 180$ mV and $V_{DDL} = 1$ V, while the DICE shift registers were functional between $V_{DDL} = 500$ mV and $V_{DDL} = 1$ V. The prototype IC is wirebonded inside a 68 pin JLCC package with a taped lid. The lid was removed during SEE testing.

B. Heavy Ion Test Facility

The radiation tests were performed at the HIF Facility at Université catholique de Louvain (UCL), Belgium. Four ion species were used for the irradiation tests. The ion species, energy, range in silicon and LET are shown in Table III. The LET values of the ions were determined using SRIM 2013 code, and are based on the composition of the interconnect layers of the IC as well as the distance to the sensitive volume, which was 11.8 μm. The same dosimetry and beam settings applied for all LET values and supply voltage settings. The flux and fluence used was approximately $15 \cdot 10^3$ ions/cm^2/s and $5 \cdot 10^6$ ions/cm^2, respectively.

C. Radiation Test Setup

The radiation test setup is shown in Fig. 8. The Device Under Test (DUT) was placed inside a vacuum chamber during radiation testing, while all the other equipment was located outside. The supply voltages V_{DDL} and V_{DDH}, were supplied to

TABLE III
ION SPECIES USED IN RADIATION TESTS

Ion species	Energy (MeV)	Range Si (μm)	LET (MeV-cm^2/mg)
$^{20}Ne^{4+}$	75	45	8.6
$^{40}Ar^{8+}$	151	40	19.4
$^{84}Kr^{17+}$	305	39	38.8
$^{124}Xe^{25+}$	420	37	53.5

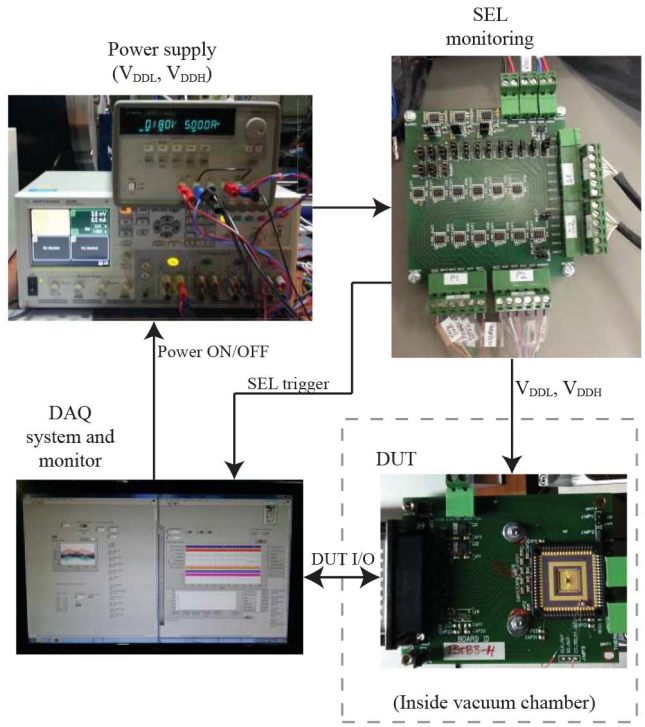

Fig. 8. Radiation test setup.

the DUT using a power supply. Prior to reaching the DUT, the supply voltage was passed through a SEL monitor, in order to detect any potential SEL in the circuitry operated at 1.2 V supply voltage. SEL was monitored separately for all the shift registers. In case of a potential SEL detection, the SEL monitoring board sends a SEL trigger to the Data Acquisition (DAQ) system, which re-cycles the power supply. The DAQ system was responsible for generating the input pattern for the shift registers as well as reading the output data and determining if an SEU has occurred. A checkerboard pattern (1-0-1 … 1-0) was clocked into the shift registers. The DAQ also provided the possibility to monitor all the DUT I/O, SEU and SEL response during irradiation testing.

A semi-static readout procedure was used in this experiment. The semi-static readout was based on writing a checkerboard pattern at 10 kHz, waiting 2 seconds and reading the shift register values (while writing a new checkerboard pattern). This procedure continued until the end of each irradiation run, which amounted to 166 readouts each time.

D. Heavy Ion Test Results

The DUT was perpendicular to the beam line for all irradiation tests (i.e. no tilt was applied). The DUT was irradiated with

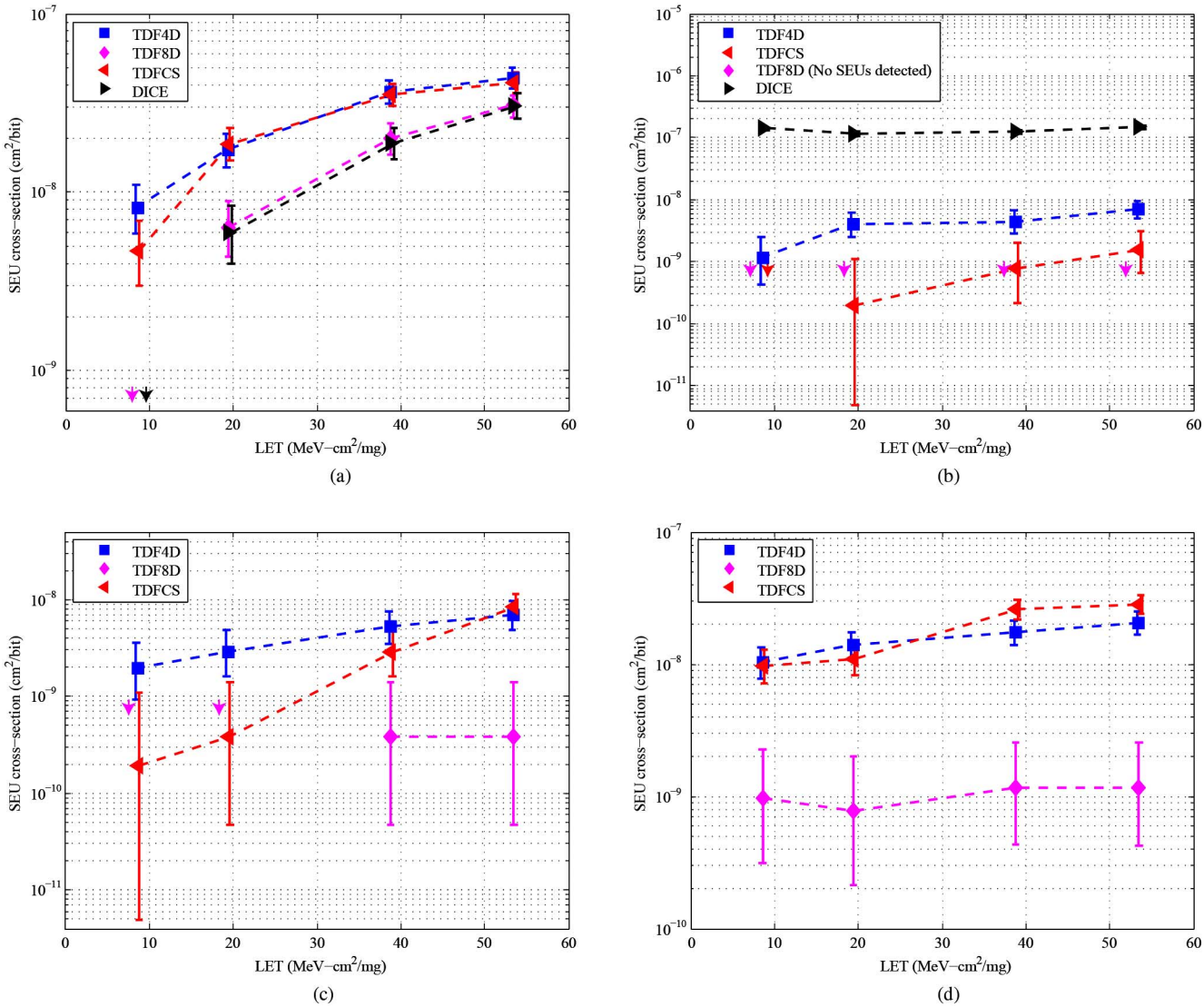

Fig. 9. SEU cross-section of TDF4D, TDF8D, TDFCS and DICE DFFs at $V_{DDL} = 1$ V, $V_{DDL} = 500$ mV, $V_{DDL} = 250$ mV, $V_{DDL} = 180$ mV. The SEU cross-section results are shown with 95% confidence interval.(a) SEU cross-section at $V_{DDL} = 1$ V.(b) SEU cross-section at $V_{DDL} = 500$ mV.(c) SEU cross-section at $V_{DDL} = 250$ mV.(d) SEU cross-section at $V_{DDL} = 180$ mV.

four ion species (LETs: 8.6, 19.4, 38.8, and 53.5) at four different supply voltages (V_{DDL}: 1 V, 500 mV, 250 mV, 180 mV). No SEL was observed in any of the irradiation tests.

Fig. 9 shows the SEU cross-section of the irradiated DFFs. In this work the SEU tolerance was evaluated by observing the SEU cross-section of the DFFs. The SEU cross-section is given by SEU cross-section $= N/(D \cdot \Phi)$, where N is the number of SEUs, Φ is the ion fluence and D is the number of DFFs in shift register. When no SEUs are observed, arrows are used to indicate the upper bound of the 95% confidence interval at that particular LET.

At a supply voltage of 1 V (Fig. 9(a)), the TDF DFFs show a relatively high SEU cross-section due to the inability of their delay elements to filter out the SETs. The DICE DFF and the TDF8D show the lowest SEU cross-section. All DFFs exhibit increasing SEU cross-section with increasing LET.

At a supply voltage of 500 mV (Fig. 9(b)), the delay elements of the TDF DFFs increase their SET filtering capability, and thereby ensure a decrease in the SEU cross-section for the TDF DFFs, compared to the SEU cross-section at 1 V supply voltage. However, in the case of the DICE DFF, an increase in the SEU cross-section was observed when scaling down the supply voltage. Among the TDF DFFs, the TDF4D has the highest SEU cross-section while the TDFCS has the second highest. At 500 mV supply voltage, no SEUs were observed in the TDF8D DFF.

At a supply voltage of 250 mV (Fig. 9(c)) the DICE DFF failed to function properly and was thereby excluded from the SEU cross-section measurements. For the TDF4D and TDFCS, similar SEU cross-section was observed compared to when $V_{DDL} = 500$ mV, however a minor increase was evident. Furthermore, in contrast to when operated at $V_{DDL} = 500$ mV, the TDFCS experiences SEUs at LET $= 8.6$ MeV-cm^2/mg. The TDF8D also exhibits an increase in the SEU cross-section compared to when $V_{DDL} = 500$ mV.

The SEU cross-section of the TDFCS and TDF4D was almost identical at $V_{DDL} = 180$ mV (Fig. 9(d)), however an increase can be observed compared to when $V_{DDL} = 250$ mV. At a supply voltage of 180 mV the TDF8D experiences SEUs across the entire LET spectrum used in the tests. It can also be seen that the SEU cross-section of the TDF8D increases compared to when $V_{DDL} = 250$ mV.

VI. Discussion

A. Radiation Tolerance Analysis

In general, all the DFFs exhibit a relatively high SEU cross-section at $V_{DDL} = 1$ V (Fig. 9(a)). In the case of the TDF DFFs, the main reason is that the delay elements do not generate long enough delay to filter out the SETs. In the case of the DICE DFF, the main reason is that the sensitive nodes are not separated far enough from each other, making these nodes sensitive to charge sharing.

As the supply voltage scales down to 500 mV (Fig. 9(b)), the increased impact of charge sharing becomes especially noticeable for the DICE DFF, where the SEU cross-section increases by a factor of 1.67 to 8.3, depending on the LET of the incident ions. However, in the case of the TDF DFFs, the delay elements generate longer delays due to the reduction in the drain-source voltage (Vds) of the transistor devices. Since longer delays are generated from the delay elements, the SETs with shorter duration than the delay elements are filtered out and cannot cause SEUs in the TDF DFFs. The SEUs which are observed in the TDF DFFs at a supply voltage of 500 mV, are partly due to ion induced SETs which have longer duration than the duration of the delay elements and partly due to charge sharing, depending on LET of the incident ions. This can be observed by comparing the SEU susceptibility of TDFCS and TDF4D. The DFTCS has longer delay duration than the TDF4D, but has shorter distance between the sensitive nodes (3.5 μm vs. 4.2 μm) compared to the TDF4D.

Due to the delay elements of the TDFCS generating longer delays than the delay elements of the TDF4D, the TDFCS has a lower SEU cross-section for LET < 38.8 MeV-cm^2/mg. However, as the LET increases, the SEU cross-section of the TDFCS approaches the SEU cross-section of the TDF4D. Since the sensitive node separation of the TDFCS is smaller than that of the TDF4D, the TDFCS becomes more sensitive to charge sharing as the LET increases. This is due to ions with higher LET generating more e-h pairs and across a large enough area to induce simultaneous charge collection at the sensitive nodes in the DFF. This trend is more prominent when the supply voltage is scaled further down to 250 mV (Fig. 9(c)). At LET < 38.8 MeV-cm^2/mg, the TDFCS has a lower SEU cross-section than the TDF4D due to the SEU cross-section being more dependent on the duration of the delay elements, and less dependent on the separation between the sensitive nodes. At LET > 38.8 MeV-cm^2/mg the SEU cross-section of TDFCS and TDF4D is similar due to the SEU cross-section being more dependent on the separation between the sensitive nodes, and less dependent on the duration of the delay elements. At LET of 53.5 MeV-cm^2/mg the SEU cross-section of the TDFCS even surpasses the SEU cross-section of the TDF4D.

At a supply voltage of 180 mV (Fig. 9(d)), the SEU cross-section of the TDF4D and the TDFCS was approximately the same. There are however small differences which also correlate with the previously mentioned observations. At LET < 38.8 MeV-cm^2/mg, the TDFCS has a slightly lower SEU cross-section than the TDF4D, while at LET > 38.8 MeV-cm^2/mg the SEU cross-section of TDFCS is now slightly higher than that of the TDF4D. Nevertheless, the SEU cross-section of both the TDFCS and the TDF4D appear to be saturated across the entire used LET spectrum. At a supply voltage of 180 mV the SEU cross-section dependency on the separation between the sensitive nodes increases compared to when the supply voltage is 250 mV. Consequently, as the supply voltage decreases, incident ions with lower LET are able to induce sufficient simultaneous charge collection on the sensitive nodes and thereby create SEUs. The TDFCS and TDF4D were also tested at a supply voltage of 150 mV for LET of 8.6 MeV-cm^2/mg and 53.5 MeV-cm^2/mg. The SEU cross-section of the TDFCS was 10% and 40% higher than the SEU cross-section of the TDF4D, for LET 8.6 MeV-cm^2/mg and 53.5 MeV-cm^2/mg, respectively.

The TDF8D showed, as expected, the highest radiation tolerance among the tested DFFs. This is due to the TDF8D having the longest input- and feedback delay as well as largest separation between the sensitive nodes. At a supply voltage of 500 mV and below, the TDF8D exhibits up to one order of magnitude lower SEU cross-section than the other TDF DFFs. At a supply voltage of 500 mV, no SEUs were observed in the TDF8D DFF. However, at a supply voltage of 250 mV and 180 mV, also the TDF8D experienced SEUs. At a supply voltage of 180 mV, similar to the other TDF DFFs, the SEU cross-section of the TDF8D also saturates, however it saturates at one order of magnitude lower than TDF4D and TDFCS.

The results indicate that at high supply voltages (> 500 mV) and low LET (< 38.8 MeV-cm^2/mg), the duration of the delay elements have the most influence on the SEU susceptibility of the TDF DFFs. On the other hand, for low supply voltages (< 500 mV) and high LET (> 38.8 MeV-cm^2/mg), the separation of the sensitive nodes has the most influence on the SEU susceptibility of the TDF DFFs. Furthermore, with decreasing supply voltage, the SEU susceptibility seems to have a lower increase with an increase in LET. A similar observation was made in [14] for FWHR transient pulsewidths.

Better SEU tolerance may be achieved by all the DFFs discussed in this paper, given that the sensitive nodes are separated with greater distance. This can be achieved by interleaving the sensitive nodes of the latches across the entire DFF [21], [22]. Furthermore, this technique can be taken one step further by interleaving sensitive nodes across several DFFs in a multi-bit register [28].

The delay of the delay elements also need to be set accordingly in order to make it possible to optimize designs in terms of radiation tolerance, performance and supply voltage. For this to be possible, SET pulsewidth characterization needs to be performed at different supply voltages. It is thereby beneficial to utilize a flexible delay elements such as the current starved inverters, which have a tunable delay. Another argument for using the current starved inverters is that standard inverter chains tend

to consume more area and energy. Based on the experimental results the current starved inverters show good SET filtering ability at different supply voltages while offering an area and energy efficient solution.

B. Radiation Testing

The irradiation tests performed in this work are based on a semi-static readout procedure. Although this procedure provides a lot of insight into the SEU behavior of the DFFs, the frequency dependency on the SEU rate could not be determined by using this readout procedure. In order to be able to characterize the frequency dependency of the SEU rate of the DFFs, a dynamic readout procedure should be used and the DFFs should be operated close to their maximum frequency.

Furthermore, due to limited beam time, only four ions were used with a fluence of $5 \cdot 10^6$ ions/cm^2. In order to gain better insight in the SEU cross-section and the $\mathrm{LET_{th}}$ of the implemented DFFs, an increased number of ions (with increased number of LETs) should have been used. Different LET values can also be achieved by utilizing different incident ion angles, which also would provide information on the charge sharing sensitivity of angled ion hits.

C. Performance

The DICE-based shift register was tested using a minimum supply voltage of 500 mV. The shift register was not able to function properly at a supply voltage of 250 mV and 180 mV. In this work, achieving high radiation tolerance was prioritized, thereby extensive efforts were not put into optimizing the electrical performance in the TDF DFFs. However, the authors are aware of several topological changes which can improve electrical performance. Having an input delay element is not critical for the SEU mitigation, as SETs appearing on the input of the TDF latch would be filtered out by the feedback delay element (given shorter SET pulsewidth than $\delta \mathrm{t_{fb}}$) and would not cause a SEU. The input delay element does help alleviate SETs on node nZ which is beneficial in terms of simultaneous multi node hits (for example simultaneous SETs on the input and node $\overline{Q}$). These events are however rare and thereby the input delay may be omitted in the TDF design without significantly sacrificing the SEU tolerance. Thereby, utilizing only the feedback delay element (with delay duration of $\delta \mathrm{t_{fb}}$) and interchanging nodes nZ and $\overline{Q}$ would remove the feedback element from the clk-to-Q delay path without significantly sacrificing SET filtering capability of the latch. These topological changes would result in a clk-to-Q delay reduction of $\delta \mathrm{t_{in}} + \delta \mathrm{t_{fb}}$ and simultaneously increase the maximum frequency of the TDF DFFs. The potential increase in the SEU susceptibility may be compensated by increasing the delay duration in the feedback delay element by $\delta \mathrm{t_{fb2}}$. The setup time would also benefit from this topological change by $\delta \mathrm{t_{in}} - \delta \mathrm{t_{fb2}}$ reduction. The area- and switching energy consumption also stand to benefit from these topological changes.

In terms of low supply voltage operation, the TDF DFFs exhibit great ability, achieving minimum supply voltages of 175 mV, 130 mV and 110 mV, for TDF8D, TDFCS and TDF4D, respectively.

VII. Conclusion

In this work, we have investigated how temporal and spatial hardening techniques influence the SEU sensitivity of DFFs as a function of a wide supply voltage range. We observe that temporal hardening has an increasing impact on the SEU sensitivity of the proposed DFF with increasing supply voltage and decreasing LET. Furthermore, we observe that spatial hardening has an increasing impact on the SEU sensitivity of the proposed DFF with decreasing supply voltage and increasing LET.

This work has also shown that temporal and spatial SEU hardening techniques in conjunction with supply voltage scaling can be used to realize low power, SEU tolerant circuits. In applications where energy efficiency is prioritized prior to operating frequency, the proposed DFF topology may be well suited for implementation. As a result, SEU cross-section of below $2 \cdot 10^{-9}$ cm^2/bit may be achieved with an increased energy efficiency of up to 95%, compared to a DICE DFF at 1 V supply voltage. Higher radiation tolerance may however be achieved by separating the sensitive nodes even further.

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